SystemVerilog
Assertions Committee
SV-AC

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SV-AC Chair

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Key Objectives for SV-AC

- Achieve a single language standard for expressing assertions in System Verilog
  - Consistent with System Verilog 3.1
- Merge in best of intersection of PSL and OVA
- Leverage system Verilog features
  - Build on DAS v1.0 baseline
- Common set of semantics for simulation, formal verification, and hybrid verification
  - Consistent results between simulation and formal verification
  - Implementable

Milestones

Milestone	orig.	Actual
• Requirements approved	9/27	10/3
• OVA donation reviewed	9/19	9/19
• OVA donation vote	9/30	10/3
• First LRM draft	12/1	
• Formal semantics review complete	3/1	
• LRM approved by SV-AC	3/1	

Status

- Requirements reviewed and voted on by SV-AC
  - Approx. 130 requirements
  - About 70 have a positive score (1 for yes –1 for no)
- OVA donation reviewed and accepted
- Draft of SVA working document presented to SV-AC
  - DWG has voted on semantics for SVA
  - Removed complex formal operators and syntax
  - Syntax being reviewed
    - Decision expected in December

Plans going forward

- Present draft SVA LRM to SV-AC (Dec 02)
- Start formal semantics review of SVA language
  - Group of volunteers from SV-AC
  - Leverage work done in PSL/OVA
  - Will not have ability to modify language only to identify technical issues for corrective purposes
- Complete LRM review in SV-AC (Feb 02)
- Final vote on SVA LRM by SV-AC (Feb 02)
- Complete formal semantics review by (Mar 03)

Review Process for SV-AC

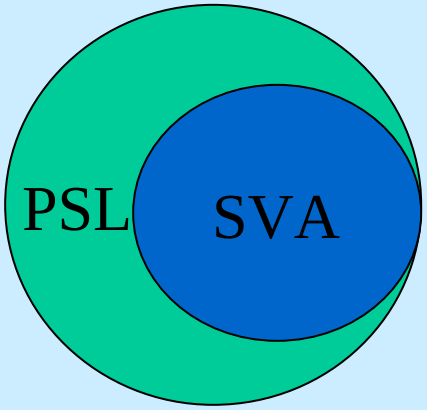
- Review LRM section by section
  - Semantics
  - Syntax
  - Code up examples to validate language
- Clocking/sampling semantics
- Booleans
- Sequences
- Properties
- Binding/instantiation
- Directives
- Templates

Issues Going Forward

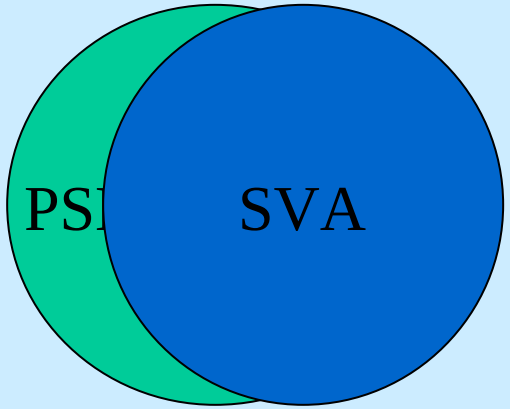
- Schedule
  - Running about two weeks behind our original schedule
  - Working to a very aggressive schedule
  - We have reduced the scope of our work significantly to help meet the schedule
- Synchronization
  - With PSL
    - We must present one consistent standard
  - With rest of System Verilog
    - Constraint specification in SV-EC

PSL vs. SVA Synchronization

- Semantic Consistency



Syntax Consistency



- Primary issue will be syntactical convergence
- PSL syntax might need to change to be consistent with SVA
- Convergence expected before SV3.1 release in June 2003