SV-EC Status
4 December 2002

David Smith – Chairman

Stefen Boyd – Co-Chairman

Agenda

- Status
- Milestones
- Plan
- Challenges

Status - Extensions

- For 3.1
  - References – being met by SV Testbench
  - Random Constraints – proposal in-review
  - Alias – approved
- Post 3.1
  - Interface Scheduling (SV-BC)
  - Interface Usage (SV-BC)
  - Modports (SV-BC)
  - Process Control
  - Data Channels
  - FSM
  - Extern Modules
  - Inferred Reg Types
  - Multi-clock/Hier FSM
  - Data Path
  - Pointers
  - Inherited Declarations
  - Force/release with strengths

Status - Issues

- Issues (from SV Testbench review)
  - 26 issues raised
  - All discussed
  - 19 issues closed
  - 7 issues will be resolved during LRM review

Status - Testbench

- Testbench LRM development
  - Many changes made due to discussions within the committee (issues and reviews)
  - First draft of 3.1 LRM with testbench is complete

Milestones

- December 15th
  - for complete integration into 3.1 LRM (Stu achieved 4th)
- December 31st
  - integration of alias and random constraints extensions in 3.1 LRM
- January 15th, 2003
  - complete review of 3.1 LRM (continue work on integration of other sections into the 3.1 LRM from SV-CC, SV-AC, SV-BC)
- February 24th, 2003
  - complete 3.1 LRM (complete at DEVCON)
- May 1, 2003
  - SV 3.1 sent to Accellera board
- June 1, 2003
  - SV 3.1 standard complete

Plan

- December 9, December 16, and January 6 2003
  - LRM Review of Testbench extensions
- January 21
  - Full day person to person meeting. LRM review of all extensions
- February 3, February 17
  - Complete LRM review for availability at DEVCON on 24 Feb
- March 17, March 31
  - Last chance for technical changes.
  - Technology freeze on March 31- only clarification and editing
- April 14, April 28
  - Clarification and editing changes
  - April 28 LRM complete and 3.1 finished at committee - pass to board

Challenges

- Support for context sensitive keywords
- Getting other committees work to integrate into 3.1 LRM