Welcome to Accellera Day!



AGENDA

- Accellera overview
- Technical Excellence Award
- Update: Accellera Portable Stimulus Working Group





Accellera Overview February 29, 2016

Shishpal Rawat | Chairman



Welcome

Agenda

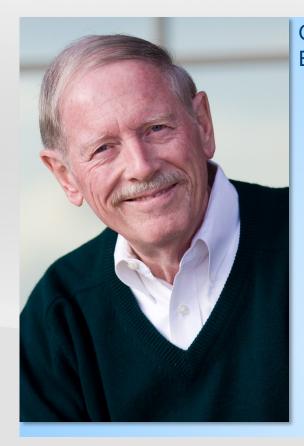
- About Accellera
- Current news
- Technical activities
- IEEE collaboration





Tribute

Remembering years of your contributions. Thank you.



Gary Smith EDA Industry Analyst 1941 - 2015

Marie Pistilli Co-founder of DAC 1933- 2015





Accellera Systems Initiative

Our Mission

To provide a platform in which the electronics industry can collaborate to innovate and deliver global standards that improve design and verification productivity for electronics products.





Broad Industry Support





Broad Industry Support

Associate Members





























































Global Presence

- DVCon U.S. March in Silicon Valley
- SystemC Evolution Day May in Munich
- DAC June in Austin
- SystemC Japan June in Shin-Yokohama
- DVCon India September in Bangalore
- DVCon Europe October in Munich



DVCon China April 2017 in Shanghai



The **SYSTEMC EVOLUTION DAY** is a user-centric technical workshop on the evolution of **SystemC-related standards** to advance **the SystemC eco-system**



Tentative Program

Lightning talks and in-depth sessions:

SystemC Parallelization & C++11/14, UVM-SystemC, CCI, TLM for serial interfaces, SystemC AMS, High-Level Synthesis

Contributions and Registration

Send your abstracts (100 words) to extend SystemC-related standards until March 31 Registration required, free of charge Location: Intel Munich (Campeon)



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DVCon is Global



www.dvcon-europe.org

www.dvcon-china.org



www.dvcon-india.org





2015-2016 Accellera News

March 2016

- Get IEEE free standards program extended 10 years/10 standards
- DVCon going to China in 2017

February 2016

Erwin de Kock receives 2016 Technical Excellence Award

October 2015

Celebrating 10 years of SystemVerilog

August 2015

SCE-MI 2.3 released

June 2015

- UVM 1.2 delivered to IEEE



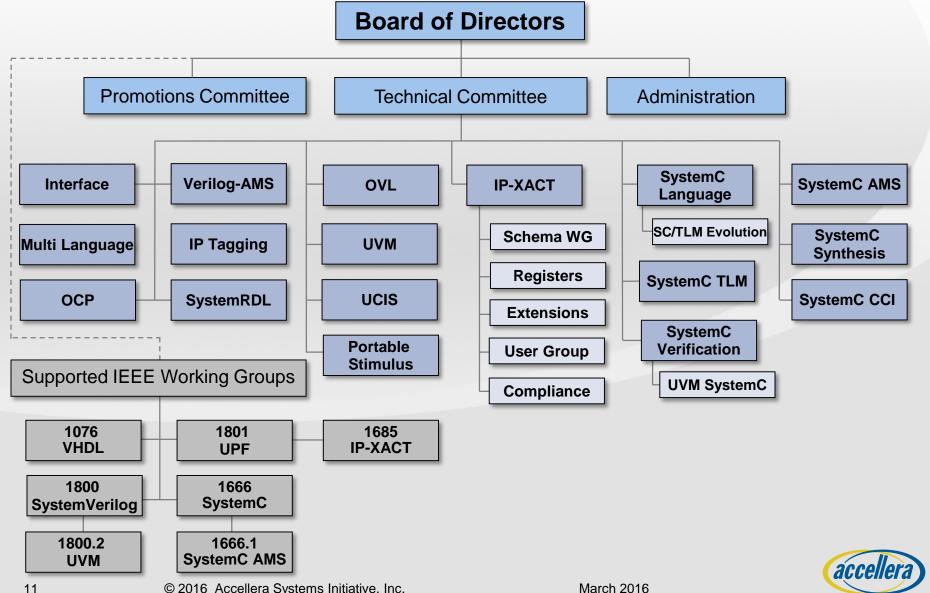
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Accellera Systems Initiative





Ongoing Technical Activities

Current Standards

- Open Verification Library (OVL) 2.8.1
- Verilog-AMS (V-AMS) 2.4
- Standard Co-Emulation Modeling Interface (SCE-MI) 2.3
- Unified Coverage Interoperability Standard (UCIS) 1.0
- IP-XACT Update of IEEE 1685 Errata and Vendor Extensions
- Intellectual Property (IP) Tagging 1.0
- Multi-Language (launched)
- Portable Stimulus (launched)
- SystemC Synthesizable Subset Draft 1.4
- SystemC Analog Mixed-Signal (AMS) 2.0
- SystemC Language and Examples 2.3.1 (includes TLM 2.0)
- SystemRDL 1.0
- Open Source Companions:
 - UVM Reference Implementation 1.2
 - SystemC Proof of Concept Library
 - SystemC Verification Library 2.0



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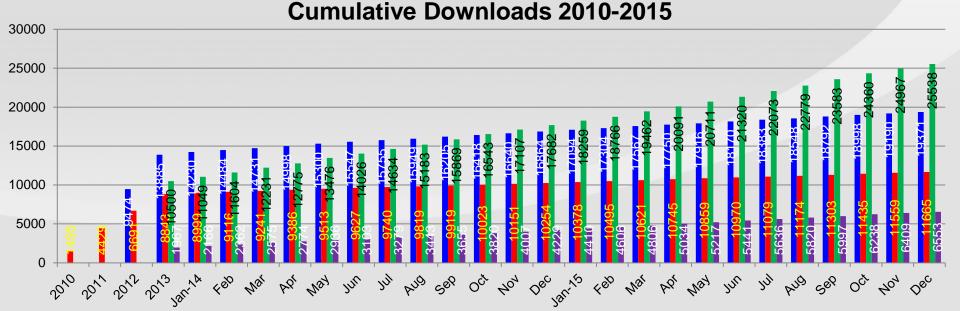
Strong Partnership with IEEE

- IEEE Get program allows access to EDA & IP standards worldwide
 - IEEE 1666 SystemC
 - IEEE 1685 IP-XACT
 - IEEE 1800 SystemVerilog
 - IEEE 1801 Unified Power Format (UPF)
- Ongoing collaboration with the IEEE Standards Association
 - 1666 SystemC Language
 - 1666.1 SystemC AMS (coming soon)
 - 1685 IP-XACT
 - 1800 SystemVerilog (SV)
 - 1800.2 UVM (coming soon)
 - 1801 Unified Power Format (UPF)
 - 1850 Property Specification Language (PSL)



IEEE Standards Access at No Charge

- Accellera relationship with the IEEE-SA
- Accellera will release <u>10 standards</u> for <u>10 years</u> under an extended
 Get IEEE program
- More than 63,000 downloads to date!



http://standards.ieee.org/about/get/

■1666 **■**1685 **■**1800 **■**1801



Advancing Standards Together

Share your experiences

- Visit www.accellera.org and register to post on forums at forums.accellera.org

Show your support

Record your adoption of standards

Become an Accellera member

- Join working groups



THANK YOU

Next: Accellera Technical Excellence Award!

- Presented by Karen Pieper, Technical Committee Chair



About the Technical Excellence Award

Accellera wishes to recognize the important achievements of its Working Group members by selecting outstanding contributors to our standards development process as recipients of the Accellera Systems Initiative Technical Excellence Award.

This annual award recognizes major contributions to the development of Accellera standards. Examples of such contributions may include leadership in standardization of new technologies, assuring achievement of standards development goals, and identifying opportunities to better serve the needs of the community through standards.



Past Recipients



2015: Justin Refice for his contribution to UVM standardization efforts.



2014: Andrew Goodrich for his contribution to SystemC standardization.



2013: Janick Bergeron for his achievements to the UVM standardization efforts.



2012: John Aynsley for his dedication to the SystemC language and community.



2016 Technical Excellence Award

- Candidates nominated by Technical Committee
- Recognizes work by people across all working groups



Erwin de Kock

Mr. de Kock is recognized for his vision and continuous efforts toward the advancement of the IP-XACT standard. IP-XACT is a standardized XML schema that defines and describes electronic components and their designs, complemented with a generator interface for design automation.



Join the DVCon Booth Crawl Tonight!



Booth Crawl Sponsors:















You won't want to miss the annual DVCon Booth Crawl on the exhibit floor. Cocktails and conversations in a casual environment with the DVCon exhibitors.

By attending the Booth Crawl you'll be automatically entered into a drawing for a \$500 VISA gift card! The winner must be present to win and will be announced tonight.

Mingle from booth to booth while enjoying food and drinks provided by participating exhibitors.



NEXT

An update from the Portable Stimulus Working Group

