>Date: Fri, 08 Nov 2002 16:45:08 -0800
>To: sv-bc@eda.org
>From: Karen Pieper <Karen.Pieper@synopsys.com>
>Subject: Agenda for 11/11/02 Meeting
>
...
>
>Action items
>Francoise is to propose text for SV-BC10: VCD and displaying enums
>Cliff is to propose examples for SV-BC10

Here is an example. Let me know if this is sufficient to satisfy SystemVerilog-BC10.

```
module fsm1 (
  // I/O declarations
  );

  enum integer (
    IDLE = 3'b000,
    S1   = 3'b001,
    S2   = 3'b011,
    S3   = 3'b111,
    ERR  = 3'b101,
    XX   = 'x    ) state, next;

  // ... fsm code
endmodule
```

Sample waveform display:

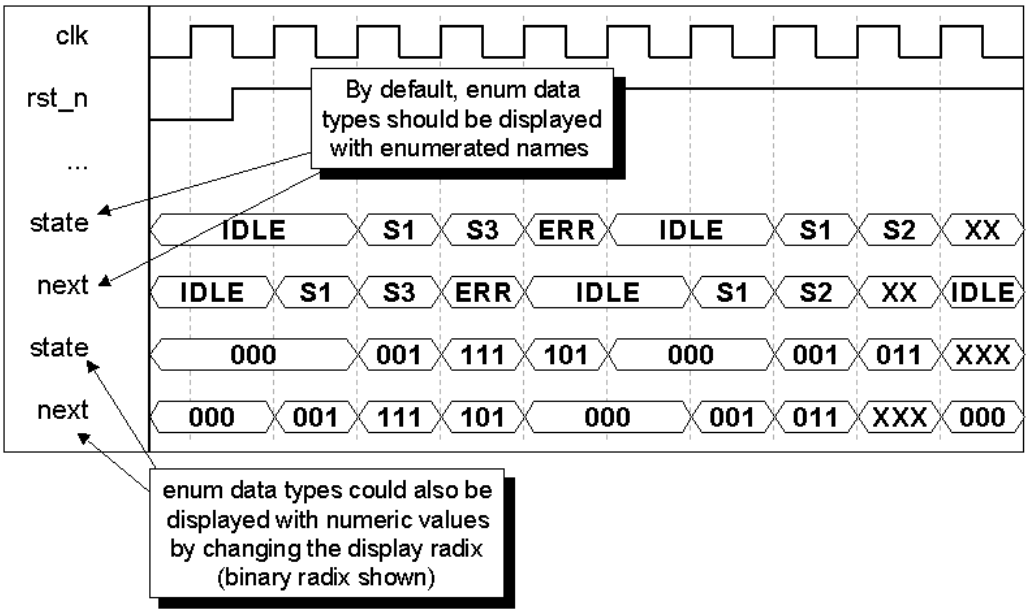

Figure 1 -Possible waveform display of enumerated types

Note that using numeric radices with unassigned enumerated names could be used to show the default values assigned by SystemVerilog compilers.

Regards - Cliff Cummings