AI-1: CH-74 handles

AI-2: CH-75 handles

AI-4: CH-76 handles

AI-5: CH-77 handles

AI-8: CH-78 handles

AI-10: Review Verilog-AMS final event, finalize the "final" proposal, and submit for review and incorporation in LRM

The Verilog_AMS final_event was reviewed. It is deemed different than what's needed for the final block. The final block specifies an entry point to procedural code whereas the AMS final-step specifies a sequence of named phases (a sequence of string literals) to be executed at the end.

CH-79 handles

AI-11: 7.5 Clarify Section 7.5 for compare and zero-filled or sign extend.
CH-82 handles

AI-12: Write up statement of process options for voting.
Added to agenda for 3 Feb 2003 meeting

AI-13: 13.2. Skew definition needs be cleaned.
AI-14: 13.2 "Clocking_event" is really a special kind of event_control (except for @*).
AI-15: 13.2 "Clarify definition of delay_expression. Is it a time variable or constant expression?

CH-80 handles all three

AI-15: 13.2: Define step. Cannot use to define timeunit or simulator time step.. Indicate impact if other modules added that change global minimum.

CH-81 handles