Fmail Voting Status

Person	I	Voting	CH-17	CH-18	CH-20	CH_47	CH-53	CH-60		CH-84		CH-86	CH-93	CH-94	CH-95	CH-96	CH-97	CH-98	CH-99	CH-100	CH-101
Arturo Salz	1																				
Brad Pierce	1																				
Cliff Cummings	1																				
Dennis Brophy	1																				
Francoise Martinolle	1		1 -13	1	1	-13	1	-13	1	-13	1	1	1	-13	1	-13	1	-13	-13	-13	3
Jay Lawrence	1		-13	1	1	1	1	-13	1	-13	1	1	-13	-13	1	-13	-13	-13	-13	-13	-13
Mehdi Mohtashemi	1																				
Neil Korpusik	1																				
Stefen Boyd	1		1 -13	1	1	1	1	-13	1	-13	1	1	1	1	1	-13	-13	1	1	-13	3 1
Stu Sutherland	1				1							1							1		1
Totals	10		3 -39	3	3	-11	1	-39	3	-39	3	3	-11	-25	3	-39	-25	-25	-25	-39	-12

1				•						1		İ								
10	;	3 -39	9 3	3	-11	1	-39) ;	3 -3	19 :	3	-11	-25	;	3 -3	9 -2	-25	-25	-39	-12
	CH-17	Jay	The persistent nature of events is still up for debate. I don't like the fact that persistent events are declared a different way (event bit) that regular events but the trigger operation is the same for persistent and regular events. There may be other ways of																	
		Francoise	accomplish					imerent way	(event bit)) that regular	events but	tne trigger o	peration is t	ne same ro	r persistent	and regular	events. There	e may be of	ner ways or	
		Stefen	As I mention	ned in http	://www.eda	.org/sv-ec/h	m/0698.htm				96.html. The	ere are signit	ficant proble	ems with th	e change p	roposed. Ins	tead of creatir	ng a new "e	vent" as the	text
	CH-18	Stefen	suggests, it									:	- 4							
	CH-16 CH-47		The bnf req											e Specific	ally conetan	t evereccio	n contains stri	na Coneta	nt evereccio	a also
	CIT-41	Tancoise															eds to be rewr			
	=.									ews are not s								-	-	
	CH-53 CH-60		Minor rewor					elleve that a	a default cid	ocking is a d	eciaration ai	nd not a state	ement. Fixe	a						
	CH-60	Jay Francoise	Definition or Replaces "If					d correspo	nds to the s	signal value	it the start o	f the verifica	tion phase.	" with: "If th	e input ske	w is zero the	n the value sa	ampled corr	esponds to	the signal
				value at the clock domain even what the clock domain even what we will are the clock domain even the clock domain even what we will do not be a second of the clock domain even																
		Stefen	We still don't know what the verification phase is yet, but assuming it resembles what we've seen, this would mean that zero skew would capture the DUT outputs 'after' NBAs have propagated. This would make sense if it was at the start of the design phase. Why does this matter? Your testbench sampling with zero delay won't won't or both zero delay rtl and gate level sims! Any clk->q delay on flops in design will mean sampling before vs after clock edge in gate vs rtl versions of dut. If we sampled at beginning of design phase, we're ok.																	
																iy on nops ii	i design			
	CH-84	Jay	Definition or			tion phase"	is TBD.													
		Francoise Stefen	ancoise Leave as it was previously said. efen same reason as CH-60																	
	CH-93	Jay		same reason as CH-ou This entire section needs to be integrated with Events and event control syntax																
	CH-94	Jay		arger issue than I want to give a quick Yes over email vote																
	Francoise Should refer to regular event control but not include it here. CH-96 Jay Much clearer but, Why aren't concatentations allowed? This still doesn't say when the drive occurs at that cycle (active event or NBA event). Is there an NBA equ												valent to this	drive?						
		Francoise	add bnf for	event_cour	nt. What abo	out using no	n blocking	drives? Do	they disapp	ear?		, ,			•					
		Stefen	The syntax allowed the						tor. There	should be a	sentence st	ating so expl	icitly, and p	resumably	there are r	estrictions o	n the kind of e	expression a	illowed? If '3	2-1' were
	CH-97	Jay	I just don't u			with bus.dat	a = ##2 - 1-1	, ,												
		Stefen															not clear if th			
			winning ass explanation		riven onto tr	ne net (no dr	iver conten	tion from m	ultiple cloci	king domain	outputs) or 1	hat each clo	cking doma	iin acts like	a driver on	the net (wh	ch is what I th	ink I remen	iber from the	e verbal
	CH-98	Jay	Definition or		of "Verifica	tion phase"	is TBD.													
	CH-99		If the the co				not for var	iables, I wo	uld insert t	he additional	proposed p	aragraph be	fore instead	d of after.						
	CH-99	Jay Francoise	How does the What is the				e: isn't bus.o	data = 0 su	pposed to	be bus.data	<= 0? I thou	aht we were	only allowing	ng 0 delav	non blockin	a drives.				
	CH-100	Jay	I like "wait fo	ork;" but no	ot exiting sin	nulation whe	n programs	s are done.	I like "disal	ble fork;" but	there is still	a bunch of t	ext here ab	out \$termir	nate() does	it belong?				
		Francoise	se I suggest that we use: wait <block_name> so that if we just name the fork parallel block we can just use that name to wait for all the spawned processes to complete. Also use: disable <block_name> to disable the fork. I don't understand the difference between \$terminate and disable. I don't see the need for \$suspend_thread if this is equivalent to a #0, just use #0.</block_name></block_name>												to disable					
		Stefen															ed to use disa	ble fork. Als	so shouldn't	compare
			against fork task setup;	, but fork <	label> form	of fork. I'm	also not sur	e that I like	"disable fo	rk" instead o	f \$terminate	() because it	t's not clear	that it wou	ld kill all chi	ld processe:	s. For example	9:		
			fork																	
				ome backg	round proce	ess of some	sort (i.e. me	onitor)												
			join_none endtask																	
			task foo; setup;																	
			fork																	
			// couple join any	things star	ted															
			disable for	k; //\$termir	nate();															
			endtask																	
							onitor from	task setup	than 'disab	le fork'. Usin	g disable is	a good idea,	though, bu	t perhaps v	ve should u	se the meth	od notation we	e've started	adopting:	
			disable.chi		ame as \$te	rminate egular disal	ale but on th	read												
	CU 404	la				tion phase"		ıı cau.												

CH-101 Jay Definition or existance of "Verification phase" is TBD. Francoise Does it mean that we are merging 13 and 14?