Proposal: Changes to section 13.1 (highlighted):

The communication between blocks of a digital system is a critical area that can affect everything from ease of RTL coding, to hardware-software partitioning, to performance analysis, to bus implementation choices and protocol checking. The interface construct in SystemVerilog was created specifically to encapsulate the communication between blocks, allowing a smooth migration from abstract system-level design through successive refinement down to lower-level register-transfer and structural views of the design. By encapsulating the communication between blocks, the interface construct also facilitates design re-use. The inclusion of ~~such a useful language feature~~interface capabilities is one of the major advantages of SystemVerilog over Verilog-2001.

?? - Do we need to add named_interface connection and ordered_interface_connection to the BNF?

Proposal: Keep the implicit port explanation and example shown in section 13.2.2 on page 59 of Draft 5.

Proposal: Keep the implicit port explanation and example shown in section 13.2.3 on page 60 of Draft 5.

Proposal: Keep the implicit port explanation shown in section 13.3 on page 61 of Draft 5.