HDL+ Minutes, June 5, 2002.
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VG: Everyone Should notice that this is an HDL+ committee Meeting.
This is not a Verilog++ committee Meeting.
The minutes are taken by Dennis Brophy.
The minutes are edited by VG. I have added Stuart Sutherland
Sorting list (I have not verified its content yet).

HDL+ Attendees
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(Vassilios to insert physical and phone attendees)

All Day Physical Attendees
Vassilios Gerousis
Harry Foster
Jayant Nagda
Bassam Tabbara
David Smith
Rich Goldman
Grant Martin
Kevin Cameron
Karen Pieper
Dennis Brophy
Paul Graham
Stuart Swan
Stuart Sutherland
Harish Chaudhry
2PM Physical Attendees
Alec
Rajiv Rarjan

Phone Attendees
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Erich Masrschenr
Karen Bartelson
Simon Davidsman
David Kelf
Adam Krolnik
Micahel McNamara
Andrew Lynch (For Michael M.)
Peter Flake
Cliff Cummings
Tom Fitzpatrick
David Lacey

HDL+ Agenda
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(See published agenda)

Introduction
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(See attached slides from Vassilios)
3.0 spec is complete; good work went to get to where we are. Thanks to all who participated in this effort.
3.1 Planning
Voting structure will depart from what was conducted for 3.0 because of influx of several representatives from several companies. Accellera

members will have voting rights, per company, and the 3.0 IEEE members will as well.

For the meeting, the following was written as a guide for the meeting:
1. Need to establish content of 3.1
2. Milestones, schedule and target need to be set
3. Committee organizational issues need to be addressed
4. Focus of SystemVerilog with 3.1 extensions.

SystemVerilog Committee Issues
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(See Vassilios' slides. Changes to the issues were updated live on his slides. Also see Stu's file of categorization of the issues created during the meeting.

New Sub-Committee
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It is proposed to create a subcommittee to prioritize the list and develop a plan to address it. Discussion on this was halted to address Simon's concerns.

Concern By Simon
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Simon stated a concern he wanted noted. It is noted in the minutes to allow the committee to reflect on this concern and serve as a formal record of it. Simon stated that 3.1's main focus was to clean and finish any issues raised with version 3.0 in order to ensure a rapid handoff to the IEEE 1364 team. He has expressed any deviation from looking only at these issues will actually not allow the team to make a deadline of 12/2002, but jeopardize the handoff of standard to the IEEE. Simon is concerned that the discussion of additional donations is out of scope with the group and that an up-front discussion of scope is appropriate and advised before discussing much more.

The concern was noted and Vassilios said the scope would be discussed as outlined in the agenda at the end of the meeting.

Synopsys Proposal
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(See Janant's slides)
Synopsys proposes enhancements to SystemVerilog with a proposal that covers:
- a) Testbench features
- b) Unified Assertions
- c) C interface
- d) Extended API

Proposal: Should SystemVerilog be limited to the Basic bucket list only?
Vote: No – Verplex, Alec (IEEE), Stu (IEEE), Synopsys, Novas, Cadence, Mentor
Yes – Cliff (IEEE), Verisity, Co-Design
Abstain – Real Intent

Motion approved

Organization Issues

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Create an issues committee to prioritize the list and to develop a plan to address the list.
Create a third sub-committee to deal with the C/C++ and interfaces with SystemVerilog
Create a subcommittee to deal with SystemVerilog language enhancements that are not in the other committees. (I.E., assertions and C/C++ I/F is not part of this group)

IEEE Plans
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The chair indicated the IEEE should start in August moving forward with the language since a lot of errata need to be addressed. Based on the good work that Accellera has done to this point, 1364 chair has delayed starting up. After errata are handled, the 1364 team would pick up in 11-12/2002 implementation experiences and corrections. If Accellera were working on other extensions, then the only other alternative open to the 1364 team would be to use 3.0 as approved and move on from that point. The 1364 chair would like to move on the committee using the IEEE owned language with the changes known today, and not have the other donations as part of it. In his duties to IEEE the chair would need to take only 3.0 and move forward and not wait for 3.1. IEEE chair suggests we look at a limited number of additions. Talking about the C interface, there are 3 PLI in the IEEEs and that should be the basis of extension, not a fourth one. The IEEE committee should be the one to take this one. Otherwise the scope will diverge from Accellera and the IEEE. It looks like a mess right here. Question to IEEE Chair: Has the committee looked at the C interface issues in the past? Yes, VPI was part of that. Synopsys did not forward Direct-C, therefore there have been no issues on this. If Synopsys would get legal to open this, then the IEEE would be open to look at it.

If we wait or give Accellera another 18 months since that is what it looks like it takes, we will not be doing our duty as an IEEE committee. I think it is time to bring it forward with these new things; lets finish what we've got.

Stu – Concurs on the PLI. Adding to the PLI really belongs on the IEEE committee. It is more than this committee can actually handle. Extending C within SystemVerilog belongs to the SystemVerilog committee.

Questions: Is IEEE 1364 looking at overlap with what the AMS is doing? Yes, but we did a poor job the last time, but they are not an IEEE standard.

Discussion: Simon - If the committee goes off to do extensions, then there is a high probability that it will not become an IEEE standard. Alec – It does not appear to be that big of a risk.

Motion: Approve creation of the sub-committees for SystemVerilog
Enhancement Committee – Vassilios Acting, but open another person
Clean-up Committee (Proposed – Cliff)
C Interface Committee - Stu

Second: Janat
Vote: No – Verisity, Co-Design

Yes – Cadence, Mentor, Synopsys, Verplex, Novas, Stu, Alec, Real Intent, Stephen Boyd
Abstained – Cliff

Motion carried.

Milestones
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First, committee needs to come back with a recommendation with a plan to prioritize what they will be doing. They will come back to the main committee and meet once a month. The sub-committee will meet as often as they can. But the first milestone should finished within 30 days after DAC.

Vassilios will meet with each of the committees to discuss what the milestones should be. The date is July 15. There will be a joint meeting on that Monday.

This discussion sounds good, but is this too many meetings?

Motion: Limit the frequency of the meetings so committee members can participate in all meetings. The time limit should be no more than 8 hours per week for meetings and must finish before 4PM Pacific Time. (Tom)

Second: Cliff

Vote: No – Synopsys Mentor
Yes – Alec, Novas, Cadence, Cliff, Verisity, Co-Design, Real Intent, Verplex, Stu, Stephen
Abstain -

Motion carried.

Categorized List
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(See Stu's list)

Assertions (OVL) Plans
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OVL Status
Rework OVL to make it more consistent and useable. Make it something that is more an IEEE standard library. The team wants to create procedural elements and currently it is concurrent. We are converting the user manual to an LRM. We are using 1.0 manual to be the base and continue this with 2.0.

OVL VHDL should have a separate committee. There is a VHDL library release, but it does not make sense to include the Verilog/Sugar in it. There are VHDL users that want to drive it participating in this work.

Sorting of Issue/Enhancement List By Stu
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Clean-up issues with 3.1 from the 5 Jun 2002 issue list:
COMMITTEE BUCKET ISSUE

BC	basic	a. Deprecation follow on
BC	basic	b. Time precision and timescale in general
BC	system	n. Dynamic process control
BC	basic	r. DSM
BC	basic	s. Data alignment and data packing issues
BC	basic	- Clarify auto increment/decrement
BC	basic	- Cadence issues w/ Section 2 literals
BC	basic	- Cadence issues w/ Section 3
BC	basic	- Section 3.1, parameterized data types
BC	basic	- Displaying enumerated types, affect on VCD
BC	basic	- Section 4: are elements of a signed packed array signed?
BC	basic	- Constant expressions
BC	basic	- Change BNF to simplify attributes--for 1364 committee?
BC	system	- Section 9: process execution efficiency
BC	basic	- Interleaving, event scheduling
BC	basic	- Constant expressions
BC	interfaces	- Interface enhancements/simplifications

Proposed Extensions to 3.1 from the 5 Jun 2002 issue list:

COMMITTEE	BUCKET	ISSUE
EC	interfaces	c. Data channels
EC	system	d. Pointers
EC	mixed-signal	e. Force/release with strengths
EC	basic	f. FSM (original ESS donation)
EC	basic	g. Extern modules
EC?	system	h. OO
EC	basic	i. Data path (possible Cadence donation)
CC	system	j. C-blend / DirectC capabilities
EC	basic	k. Alias
EC	basic	l. Inherited declarations
EC	basic	m. Multi-clock FSM
CC	system	o. API/PLI
AC	verification	p. Temporal logic
EC	basic	q. Inferred reg types

BC = Basic Committee (primarily clarifications & minor extensions to 3.0 LRM)
EC = Enhancement Committee (primarily modeling enhancements to 3.0 LRM)
CC = C/C++ Committee (primarily C language, API, PLI enhancements to 3.0 LRM)
AC = Assertions Committee (primarily verification enhancements to 3.0 LRM)